Atty. Docket No.: M-8353 US
1st Inventor: Douglas Duschatko
Attorney: Jack V. Musgrove
Phone No.: (512) 794-3600

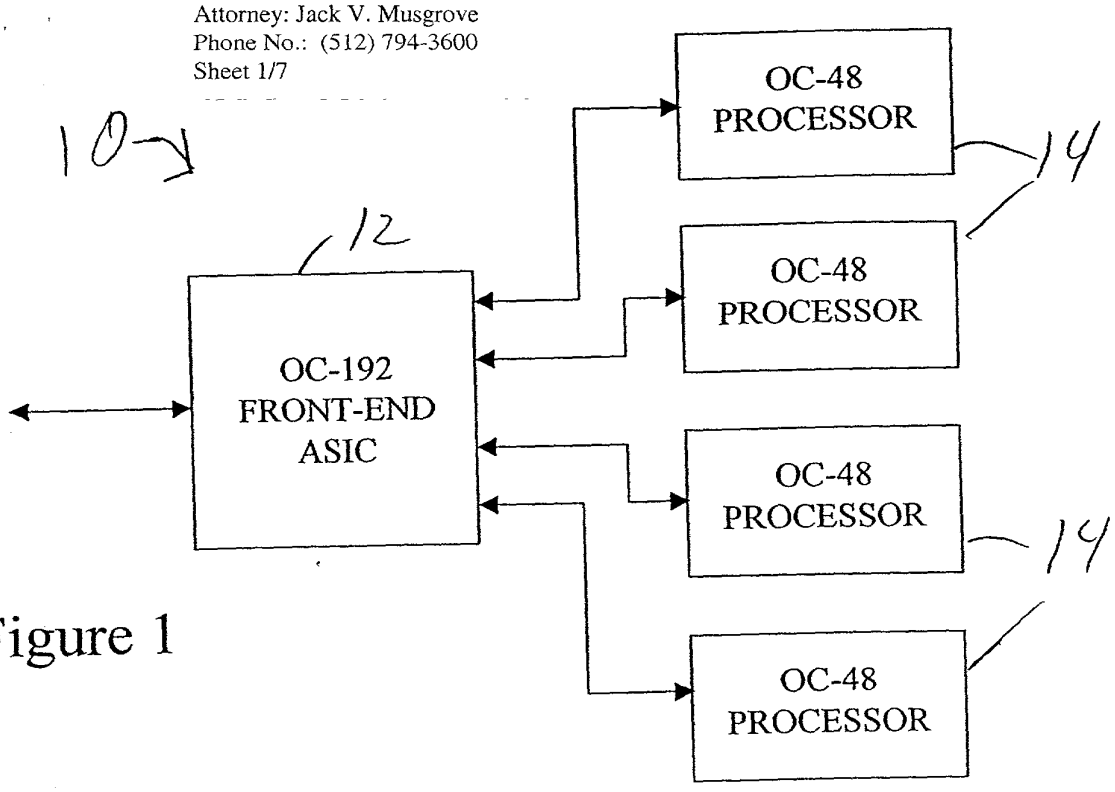

Figure 1

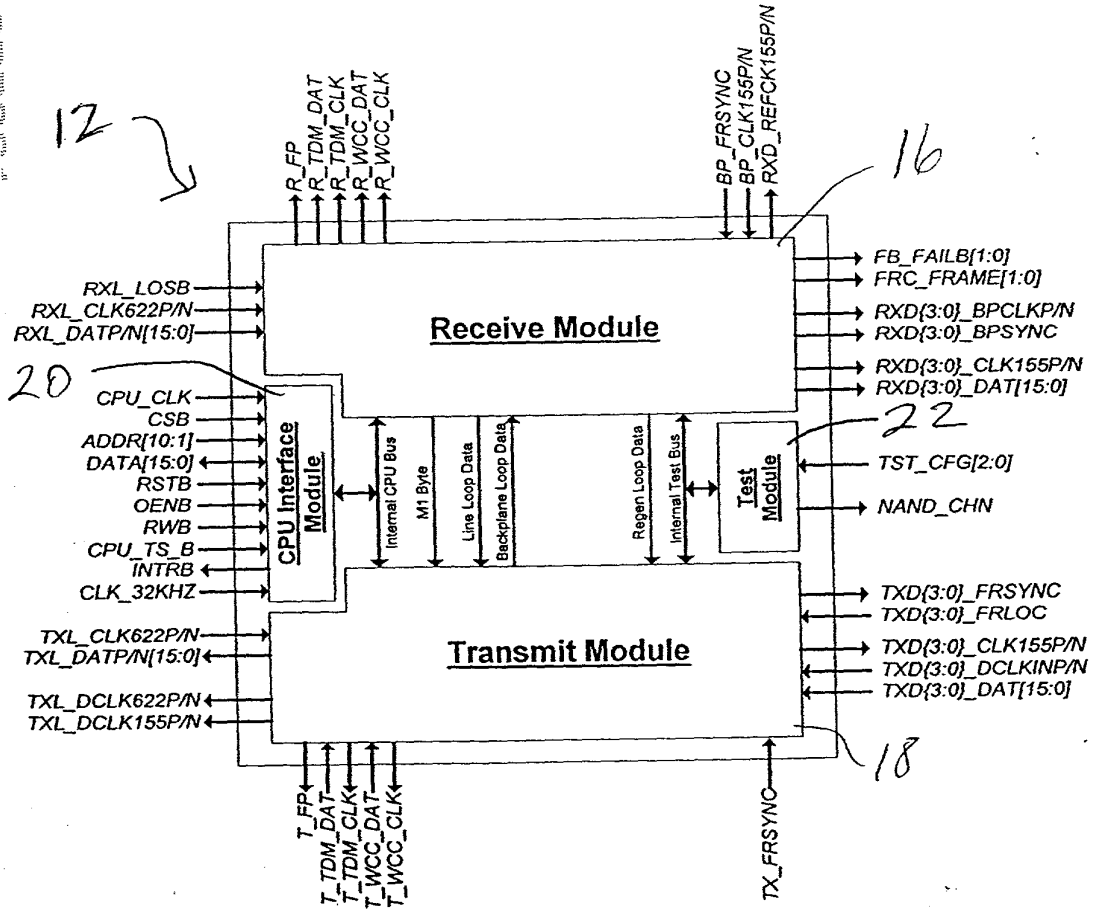

Fig. 2

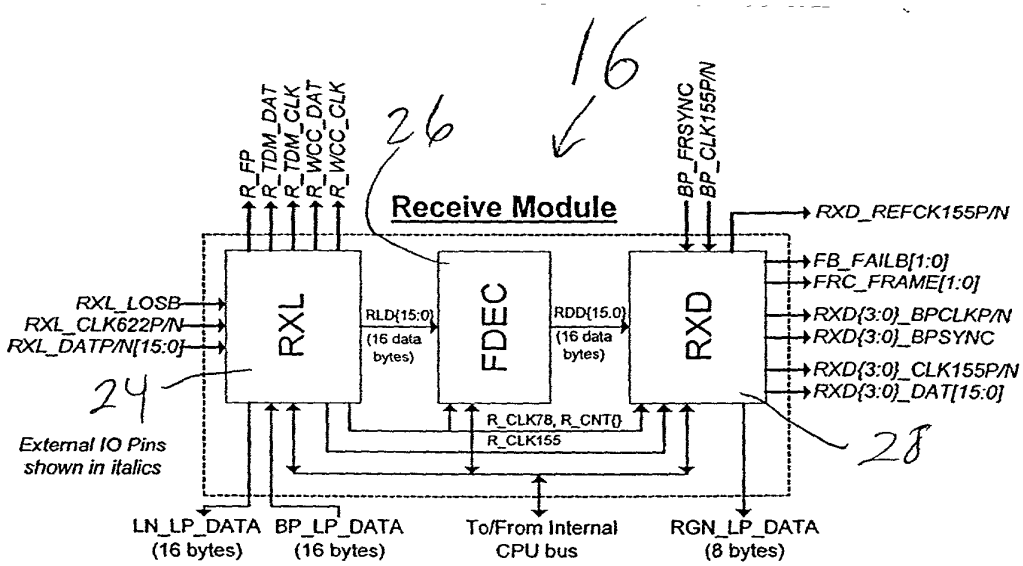
16
26
Receive Module
R_FP
R_TDM_DAT
R_TDM_CLK
R_WCC_DAT
R_WCC_CLK
BP_FRSYNC
BP_CLK155P/N
RXD_REFCK155P/N
RXL_LOSB
RXL_CLK622P/N
RXL_DATP/N[15:0]
RXL
RLD{15:0}
(16 data bytes)
FDEC
RDD{15.0}
(16 data bytes)
RXD
FB_FAILB[1:0]
FRC_FRAME[1:0]
RXD{3:0}_BPCLKP/N
RXD{3:0}_BPSYNC
RXD{3:0}_CLK155P/N
RXD{3:0}_DAT[15:0]
24
External IO Pins shown in italics
R_CLK78, R_CNT{}
R_CLK155
28
LN_LP_DATA (16 bytes)
BP_LP_DATA (16 bytes)
To/From Internal CPU bus
RGN_LP_DATA (8 bytes)

Fig. 3

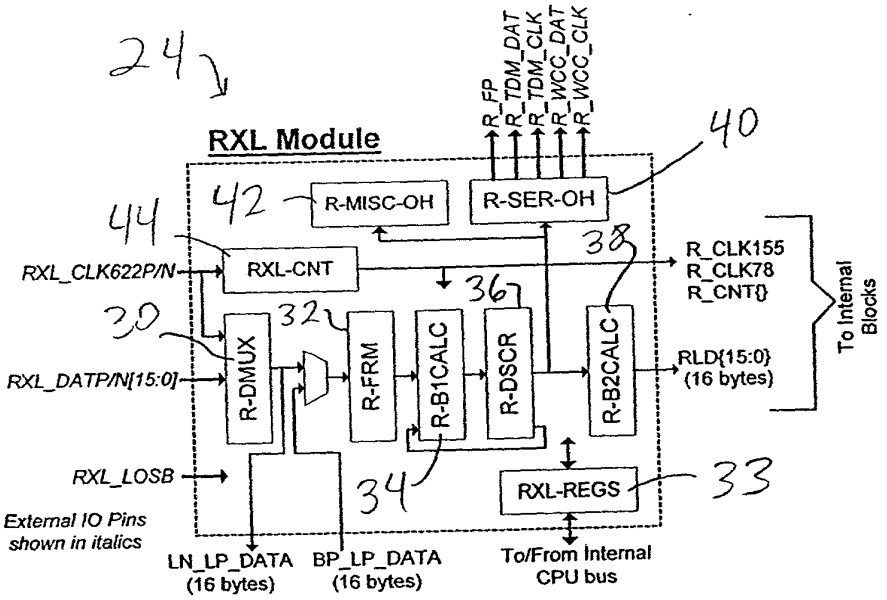
24
RXL Module
R_FP
R_TDM_DAT
R_TDM_CLK
R_WCC_DAT
R_WCC_CLK
40
42
R-MISC-OH
R-SER-OH
44
38
RXL_CLK622P/N
RXL-CNT
R_CLK155
R_CLK78
R_CNT{}
36
30
32
RXL_DATP/N[15:0]
R-DMUX
R-FRM
R-B1CALC
R-DSCR
R-B2CALC
RLD{15:0} (16 bytes)
To Internal Blocks
RXL_LOSB
34
RXL-REGS
33
External IO Pins shown in italics
LN_LP_DATA (16 bytes)
BP_LP_DATA (16 bytes)
To/From Internal CPU bus

Fig. 4

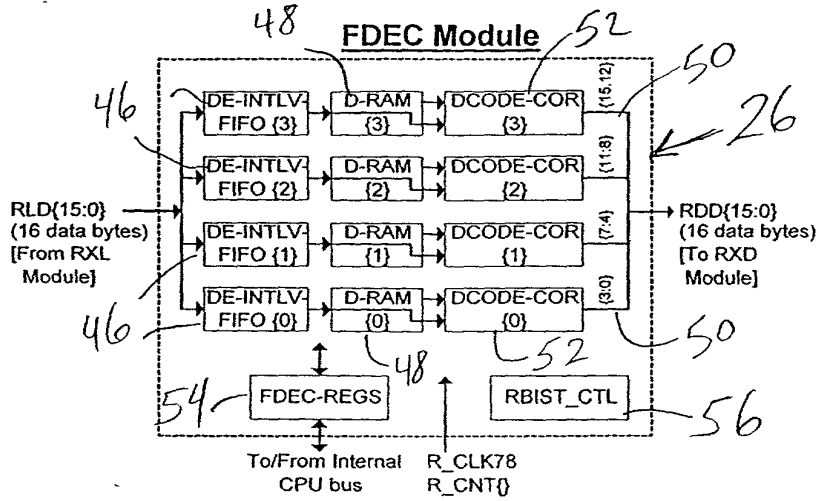
FDEC Module
48
52
50
46
26
DE-INTLV FIFO {3}
D-RAM {3}
DCODE-COR {3}
DE-INTLV FIFO {2}
D-RAM {2}
DCODE-COR {2}
DE-INTLV FIFO {1}
D-RAM {1}
DCODE-COR {1}
DE-INTLV FIFO {0}
D-RAM {0}
DCODE-COR {0}
{15:12}
{11:8}
{7:4}
{3:0}
RLD{15:0}
(16 data bytes)
[From RXL Module]
RDD{15:0}
(16 data bytes)
[To RXD Module]
FDEC-REGS
RBIST_CTL
54
56
To/From Internal CPU bus
R_CLK78
R_CNT{}

Fig. 5

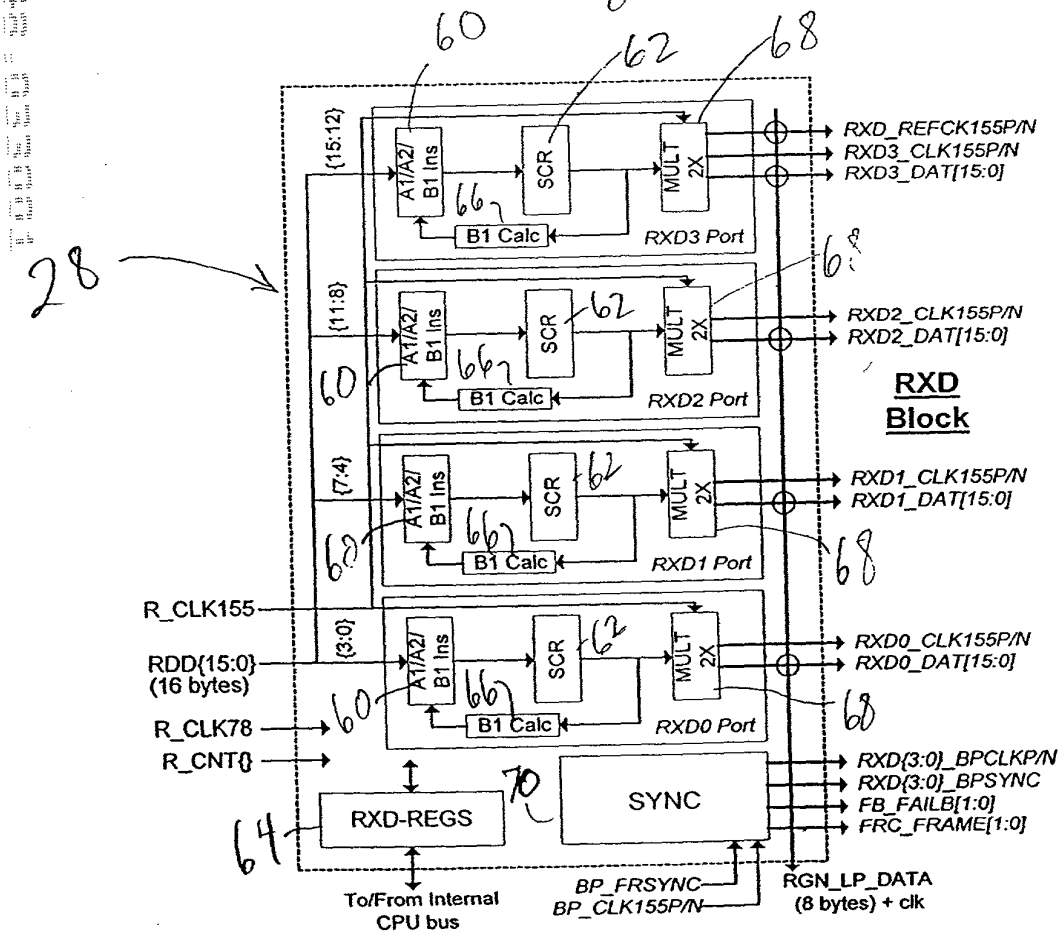
28
60
62
68
A1/A2/ B1 Ins
SCR
MULT 2X
B1 Calc
RXD3 Port
RXD2 Port
RXD1 Port
RXD0 Port
RXD_REFCK155P/N
RXD3_CLK155P/N
RXD3_DAT[15:0]
RXD2_CLK155P/N
RXD2_DAT[15:0]
RXD1_CLK155P/N
RXD1_DAT[15:0]
RXD0_CLK155P/N
RXD0_DAT[15:0]
RXD Block
R_CLK155
RDD{15:0}
(16 bytes)
R_CLK78
R_CNT{}
RXD-REGS
SYNC
64
70
RXD{3:0}_BPCLKP/N
RXD{3:0}_BPSYNC
FB_FAILB[1:0]
FRC_FRAME[1:0]
To/From Internal CPU bus
BP_FRSYNC
BP_CLK155P/N
RGN_LP_DATA
(8 bytes) + clk

FIG. 6

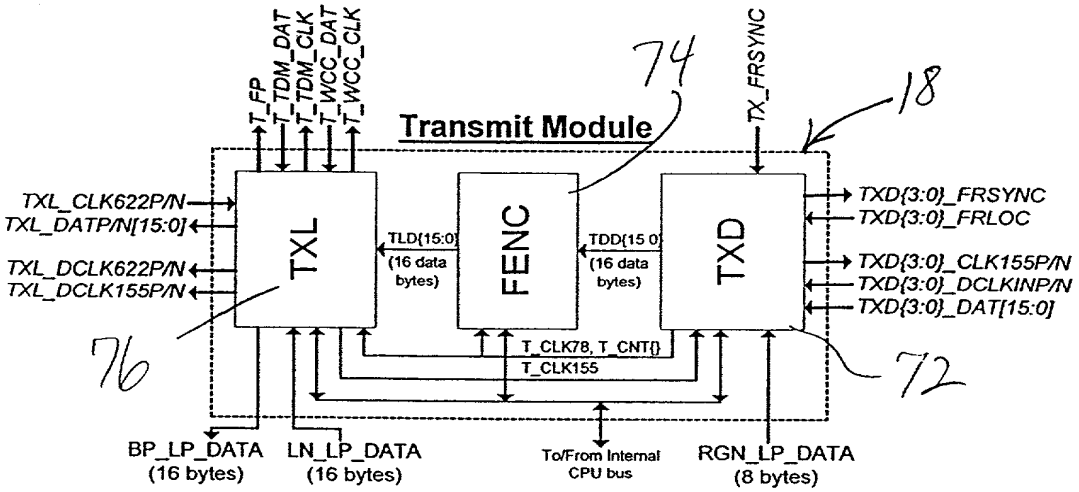
T_FP
T_TDM_DAT
T_TDM_CLK
T_WCC_DAT
T_WCC_CLK
Transmit Module
74
18
TX_FRSYNC
TXL_CLK622P/N
TXL_DATP/N[15:0]
TXL_DCLK622P/N
TXL_DCLK155P/N
TXL
TLD{15:0}
(16 data bytes)
FENC
TDD{15:0}
(16 data bytes)
TXD
TXD{3:0}_FRSYNC
TXD{3:0}_FRLOC
TXD{3:0}_CLK155P/N
TXD{3:0}_DCLKINP/N
TXD{3:0}_DAT[15:0]
T_CLK78, T_CNT{}
T_CLK155
76
72
BP_LP_DATA
(16 bytes)
LN_LP_DATA
(16 bytes)
To/From Internal CPU bus
RGN_LP_DATA
(8 bytes)

Fig. 7

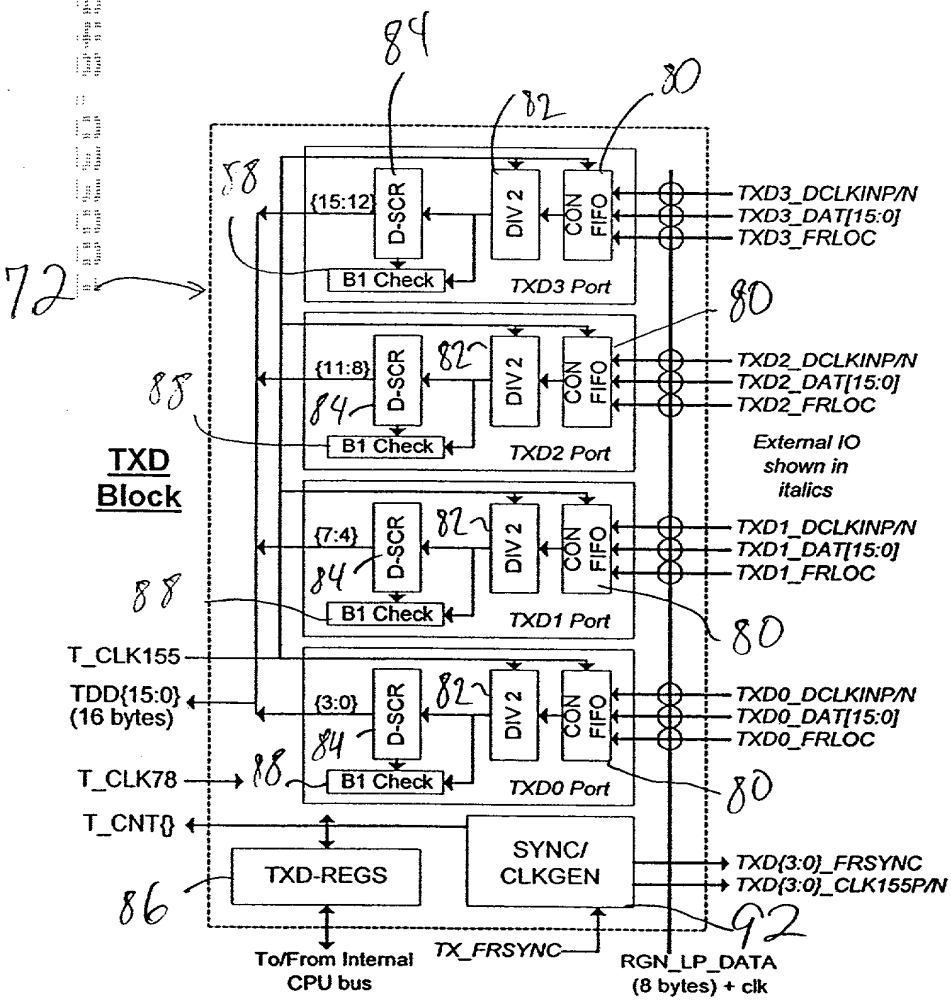
84
82
80
88
72
{15:12}
D-SCR
DIV 2
CON FIFO
B1 Check
TXD3 Port
TXD3_DCLKINP/N
TXD3_DAT[15:0]
TXD3_FRLOC
{11:8}
TXD2 Port
TXD2_DCLKINP/N
TXD2_DAT[15:0]
TXD2_FRLOC
85
External IO shown in italics
TXD Block
{7:4}
TXD1 Port
TXD1_DCLKINP/N
TXD1_DAT[15:0]
TXD1_FRLOC
{3:0}
TXD0 Port
TXD0_DCLKINP/N
TXD0_DAT[15:0]
TXD0_FRLOC
T_CLK155
TDD{15:0} (16 bytes)
T_CLK78
T_CNT{}
TXD-REGS
SYNC/ CLKGEN
TXD{3:0}_FRSYNC
TXD{3:0}_CLK155P/N
86
92
To/From Internal CPU bus
TX_FRSYNC
RGN_LP_DATA
(8 bytes) + clk

Fig. 8

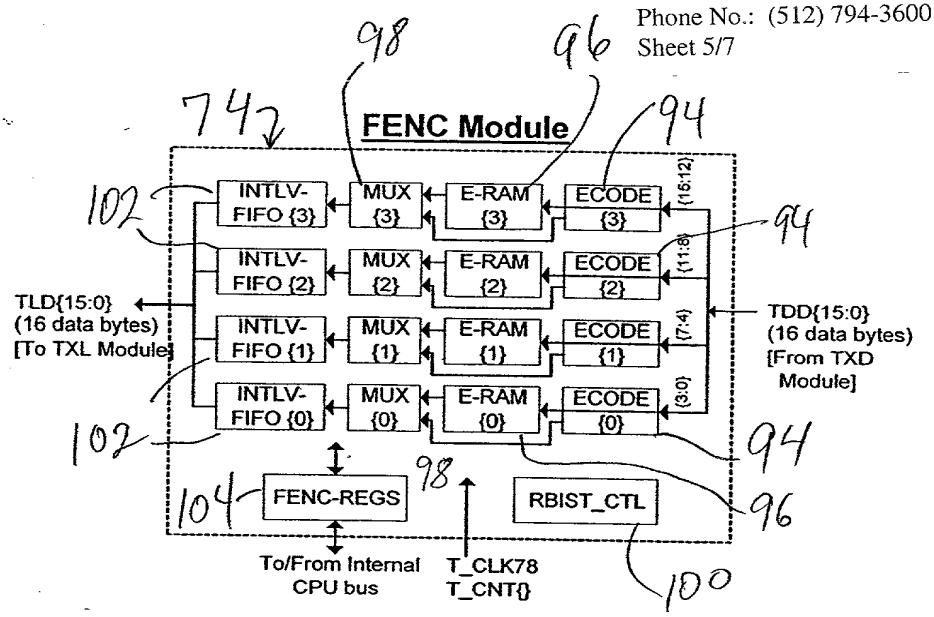
FENC Module
INTLV-FIFO {3}
MUX {3}
E-RAM {3}
ECODE {3}
INTLV-FIFO {2}
MUX {2}
E-RAM {2}
ECODE {2}
INTLV-FIFO {1}
MUX {1}
E-RAM {1}
ECODE {1}
INTLV-FIFO {0}
MUX {0}
E-RAM {0}
ECODE {0}
{15:12}
{11:8}
{7:4}
{3:0}
TLD{15:0}
(16 data bytes)
[To TXL Module]
TDD{15:0}
(16 data bytes)
[From TXD Module]
FENC-REGS
RBIST_CTL
To/From Internal CPU bus
T_CLK78
T_CNT{}
98
96
94
102
104
100

Fig. 9

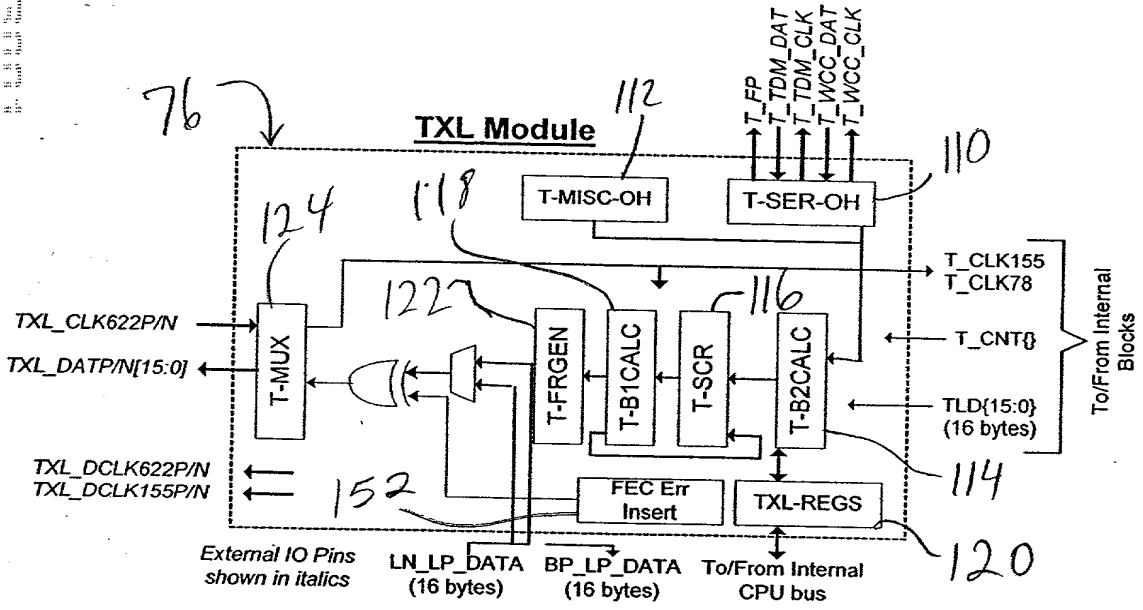
TXL Module
T_FP
T_TDM_DAT
T_TDM_CLK
T_WCC_DAT
T_WCC_CLK
T-MISC-OH
T-SER-OH
T_CLK155
T_CLK78
T_CNT{}
TLD{15:0}
(16 bytes)
To/From Internal Blocks
TXL_CLK622P/N
TXL_DATP/N[15:0]
T-MUX
T-FRGEN
T-B1CALC
T-SCR
T-B2CALC
TXL_DCLK622P/N
TXL_DCLK155P/N
FEC Err Insert
TXL-REGS
External IO Pins shown in italics
LN_LP_DATA
(16 bytes)
BP_LP_DATA
(16 bytes)
To/From Internal CPU bus
76
112
110
124
118
122
116
114
152
120

Fig. 10

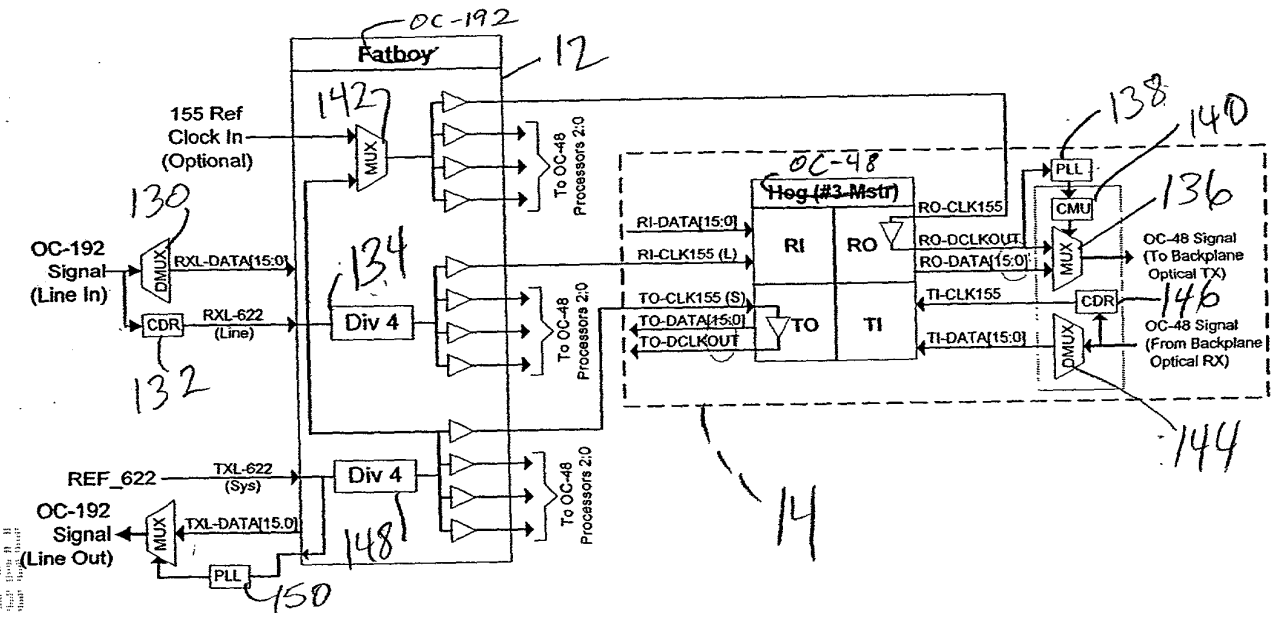

Fig. 11

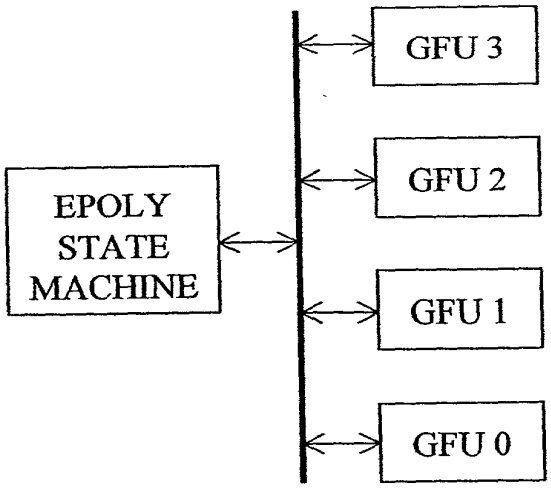

Figure 12

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Sheet 7/7

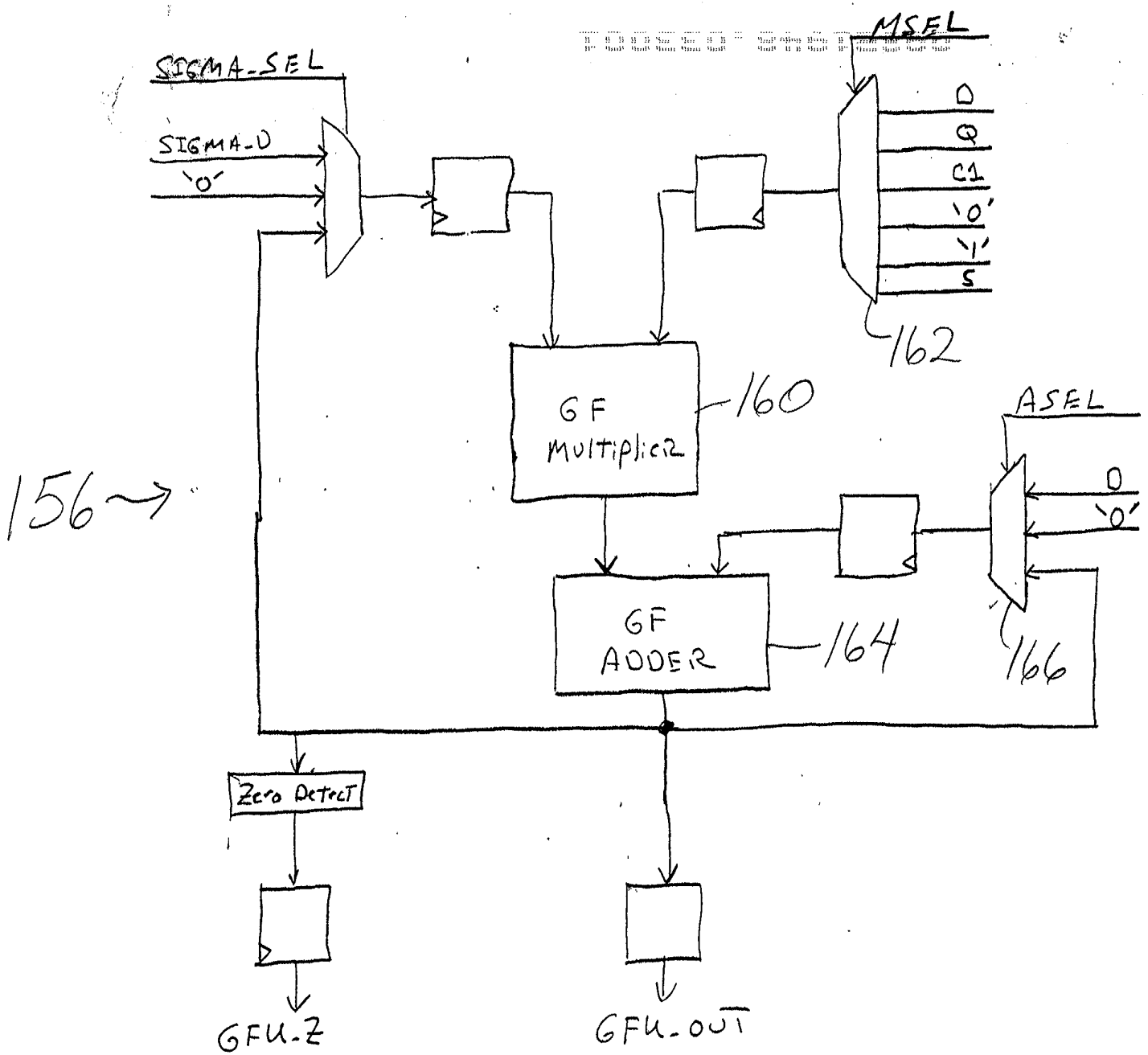

Fig. 13